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<th>Kurskod</th>
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<th>Tentamensdatum</th>
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<tr>
<td>ETO60G</td>
<td>1101</td>
<td>2019-03-20</td>
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<tr>
<td>Elektroteknik GR (A) Digitalteknik med VHDL</td>
<td>Tentamen - Sundsvall</td>
<td>Sundsvall</td>
<td>VT2019</td>
<td>Elektroteknik</td>
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Digitalteknik med VHDL

Time | 5 hours
Support material | none
No. of questions | 6
No. of pages | 4
No. of points | 50 (25 for passed)

- Please hand in one task per page.
- Rationale may not be so scarce that they become difficult to follow.
- Reasoning behind equations should be explained.
- Calculations shall be sufficiently complete to show how the result was obtained.
- Each task must be concluded with a clearly written answer.

David Krapohl, tel: 010-142 8755, e-post: david.krapohl@miun.se
Tasks

Exercise 1.
   a) Convert the following hexadecimal number to octal and binary notation:  
      \[ 16e.c_{16} \]  
      2 P.
   b) Use the left-shift operation to calculate the binary result of:  
      \[ 10100011_2 \times 5_{10} \]  
      2 P.
   c) Calculate \(-3 - 7\) with two's complement using 8 bit registers.  
      3 P.

Exercise 2.
   a) Determine if the following equality is true:  
      \[ a \cdot \overline{b} + a \cdot \overline{c} + \overline{a} \cdot b = (a \cdot b \cdot c) \cdot (\overline{a} \cdot \overline{b}) \]  
      4 P.
   b) Minimise the following Boolean equation:  
      \[ (a + b) + (a \cdot c) + (b \cdot \overline{c}) \cdot (b + c) \]  
      4 P.
   c) Minimise the function \( f(abcd) = \Sigma(0,5,7,8,11,13,15) + d(2,10,14) \) with the help of a Karnaugh-map. Draw a gate level diagram for the minimised expression.  
      5 P.

Exercise 3.
Develop Boolean expressions that model the behaviour of the state machine below.  
Use binary coding and D-flipflops.
Exercise 4.
Draw a gate level diagram for the equation below and complete the waveform output for X.

\[ X = AB + \overline{AB} + CD + DE + \overline{BC} \]  
(1)

Exercise 5.
Write the truth table and draw the gate level diagram for a 2-4-decoder. Complete the VHDL code below to achieve the same functionality.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity decoder24 is
port(
a : in STD_LOGIC_VECTOR(1 downto 0);
b : out STD_LOGIC_VECTOR(3 downto 0)
);
end decoder24;

architecture behaviour of decoder24 is
begin
-----------------------------
-- <<<write your code here>>>
-----------------------------
end behaviour;
```

Exercise 6.
a) Draw or describe the signal behaviour for A, B and C with respect to delta delay when the input signal switches from 1 to 0.

4 P.
b) Calculate the maximum gate delay path for the following gate level circuit with the given delays.

\[ \begin{array}{c|c|c|c|c} \text{Gates} & \text{Delay} \\
\hline \text{inverter} & 0.1\text{ns} \\
\text{nand} & 0.4\text{ns} \\
\text{and} & 0.9\text{ns} \\
\text{or} & 0.3\text{ns} \\
\end{array} \]