



Försättsblad Prov Original

Kurskod	Provkod	Tentamensdatum
E T 0 6 0 G	I 1 0 1	2 0 1 9 - 0 3 - 2 0
Kursnamn	Elektroteknik GR (A) Digitalteknik med VHDL	
Provnamn	Tentamen - Sundsvall	
Ort	Sundsvall	
Termin	VT2019	
Ämne	Elektroteknik	



Mittuniversitetet
MID SWEDEN UNIVERSITY

Exam – ET060G/ET061G – 20 March 2019

Digitalteknik med VHDL

Time	5 hours
Support material	none
No. of questions	6
No. of pages	4
No. of points	50 (25 for passed)

- Please hand in one task per page.
- Rationale may not be so scarce that they become difficult to follow.
- Reasoning behind equations should be explained.
- Calculations shall be sufficiently complete to show how the result was obtained.
- Each task must be concluded with a clearly written answer.

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Tasks

Exercise 1.

- a) Convert the following hexadecimal number to octal and binary notation: 2 P.

$$16e.c_{16}$$

- b) Use the left-shift operation to calculate the binary result of: 2 P.

$$10100011_2 \times 5_{10}$$

- c) Calculate $-3 - 7$ with two's complement using 8 bit registers. 3 P.

Exercise 2.

- a) Determine if the following equality is true: 4 P.

$$a \cdot \bar{b} + a \cdot \bar{c} + \bar{a} \cdot b = \overline{(a \cdot b \cdot c)} \cdot \overline{(\bar{a} \cdot \bar{b})}$$

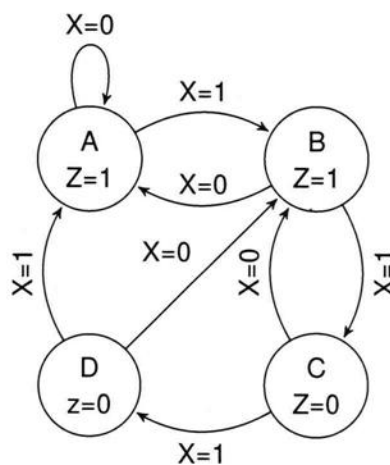
- b) Minimise the following Boolean equation: 4 P.

$$(a + b) + (a \cdot c) + \overline{(b \cdot \bar{c}) \cdot (b + c)}$$

- c) Minimise the function $f(abcd) = \sum(0, 5, 7, 8, 11, 13, 15) + d(2, 10, 14)$ with the help of a Karnaugh-map. Draw a gate level diagram for the minimised expression. 5 P.

Exercise 3.

Develop Boolean expressions that model the behaviour of the state machine below. 6 P.
Use binary coding and D-flipflops.

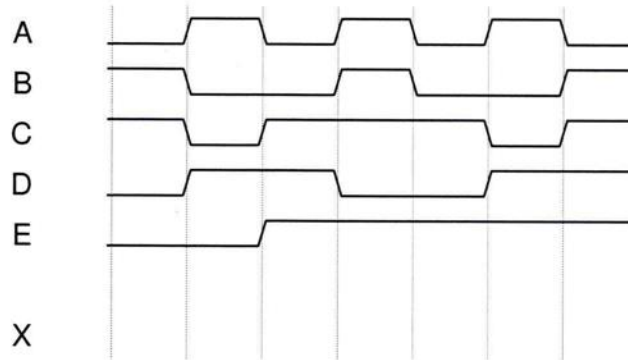


Exercise 4.

Draw a gate level diagram for the equation below and complete the waveform output for X.

$$X = AB + \bar{A}B + C\bar{D} + D\bar{E} + \bar{B}C \quad (1)$$

4 P.



4 P.

Exercise 5.

Write the truth table and draw the gate level diagram for a 2-4-decoder. Complete the VHDL code below to achieve the same functionality. 9 P.

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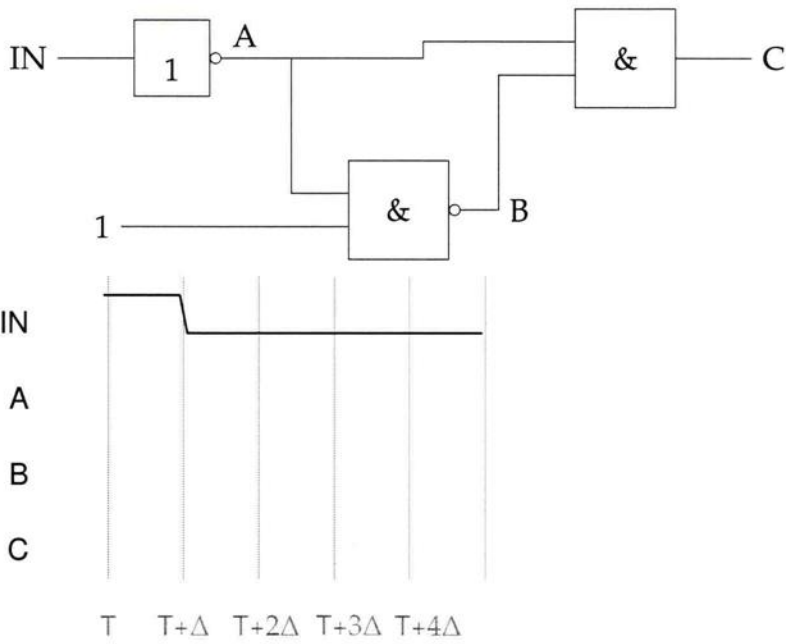
1      library IEEE;
2      use IEEE.STD_LOGIC_1164.all;
3
4      entity decoder24 is
5          port(
6              a : in STD_LOGIC_VECTOR(1 downto 0);
7              b : out STD_LOGIC_VECTOR(3 downto 0)
8          );
9      end decoder24;
10
11     architecture behaviour of decoder24 is
12     begin
13         -----
14         -- <<<write your code here>>>
15         -----
16     end behaviour;

```

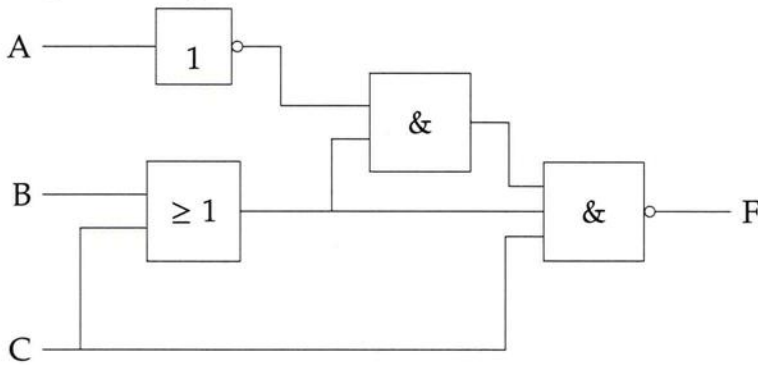
Exercise 6.

- a) Draw or describe the signal behaviour for A, B and C with respect to delta delay when the input signal switches from 1 to 0.

4 P.



b) Calculate the maximum gate delay path for the following gate level circuit with the given delays. 3P.



Gates Delay	
inverter	0.1ns
nand	0.4ns
and	0.9ns
or	0.3ns