<table>
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<th>Kurskod</th>
<th>Provkod</th>
<th>Tentamensdatum</th>
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<tbody>
<tr>
<td>ET061G</td>
<td>T101</td>
<td>2019-03-20</td>
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<tr>
<td>Elektroteknik GR (A), Digitalteknik med VHDL</td>
<td>Tentamen - Sundsvall</td>
<td>Sundsvall</td>
<td>VT2019</td>
<td>Elektroteknik</td>
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Exam - ET060G/ET061G – 20 March 2019

Digitalteknik med VHDL

<table>
<thead>
<tr>
<th>Time</th>
<th>5 hours</th>
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<tbody>
<tr>
<td>Support material</td>
<td>none</td>
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<tr>
<td>No. of questions</td>
<td>6</td>
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<tr>
<td>No. of pages</td>
<td>4</td>
</tr>
<tr>
<td>No. of points</td>
<td>50 (25 for passed)</td>
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• Please hand in one task per page.
• Rationale may not be so scarce that they become difficult to follow.
• Reasoning behind equations should be explained.
• Calculations shall be sufficiently complete to show how the result was obtained.
• Each task must be concluded with a clearly written answer.

David Krapohl, tel: 010-142 8755, e-post: david.krapohl@miun.se
Tasks

Exercise 1.
   a) Convert the following hexadecimal number to octal and binary notation: 2 P.
       \[ 16c.c_{16} \]
   b) Use the left-shift operation to calculate the binary result of: 2 P.
       \[ 10100011_2 \times 5_{10} \]
   c) Calculate \(-3 - 7\) with two's complement using 8 bit registers. 3 P.

Exercise 2.
   a) Determine if the following equality is true: 4 P.
       \[ a \cdot \overline{b} + a \cdot \overline{c} + \overline{a} \cdot b = (a \cdot b \cdot c) \cdot (\overline{a} \cdot \overline{b}) \]
   b) Minimise the following Boolean equation: 4 P.
       \[ (a + b) + (a \cdot c) + (b \cdot \overline{c}) \cdot (b + c) \]
   c) Minimise the function \( f(abc) = \sum(0, 5, 7, 8, 11, 13, 15) + d(2, 10, 14) \) with the help of a Karnaugh-map. Draw a gate level diagram for the minimised expression. 5 P.

Exercise 3.
Develop Boolean expressions that model the behaviour of the state machine below. 6 P.
Use binary coding and D-flipflops.

![State machine diagram]
Exercise 4.
Draw a gate level diagram for the equation below and complete the waveform output for X.

\[ X = AB + \overline{A}B + C\overline{D} + DE + \overline{B}C \]  

4P.

Exercise 5.
Write the truth table and draw the gate level diagram for a 2-4-decoder. Complete the VHDL code below to achieve the same functionality.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity decoder24 is
  port(
    a : in STD_LOGIC_VECTOR(1 downto 0);
    b : out STD_LOGIC_VECTOR(3 downto 0)
  );
end decoder24;

architecture behaviour of decoder24 is
begin
  -- <<<write your code here>>>
end behaviour;
```

9P.

Exercise 6.
a) Draw or describe the signal behaviour for A, B and C with respect to delta delay when the input signal switches from 1 to 0.  
4P.
b) Calculate the maximum gate delay path for the following gate level circuit with the given delays.

\[
\begin{array}{c}
\text{IN} \\
1 \\
\text{A} \\
\text{B} \\
\text{C} \\
T \quad T+\Delta \quad T+2\Delta \quad T+3\Delta \quad T+4\Delta
\end{array}
\]

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<tr>
<th>Gates</th>
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<tbody>
<tr>
<td>inverter</td>
<td>0.1ns</td>
</tr>
<tr>
<td>nand</td>
<td>0.4ns</td>
</tr>
<tr>
<td>and</td>
<td>0.9ns</td>
</tr>
<tr>
<td>or</td>
<td>0.3ns</td>
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